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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,947	10/30/2000	Edmund J. Kelly	TRANS04D	8830

7590 01/14/2002
Stephen L. King
30 Sweetbay Road
Rancho Palos Verdes, CA 90275

EXAMINER

THAI, TUAN V

ART UNIT	PAPER NUMBER
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2186

DATE MAILED: 01/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/699,947	KELLY ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2000.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-9,12,13 and 18-20 is/are pending in the application.
- 4a) Of the above claim(s) 4,10,11 and 14-17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-9,12,13 and 18-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other:

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Part III DETAILED ACTION

Specification

1. This application is a continuation of application 08/702,771 filed August 22, 1996; now U.S. Patent 6,199,152. Claims 1-3, 5-9, 12-13 and 18-20 are presented for examination. Claims 4, 10-11 and 14-17 have been cancelled.
2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Double Patenting

3. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

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4. Claims 1-3, 5-9, 12-13 and 18-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of U.S. Patent No. 6,199,152. Although the conflicting claims are not identical, they are not patentably distinct from each other because the wording of the instant claims are broader as compared to the limitations of the original claims. The instant claims are slightly broader in their new form. Examples are: Claims 1, 7, 12 and 18 of the current application are obvious slight variation of claims 1-5 and 7 of patent 6,199,152. The claims are not patentably distinct from each other because they are directed to the same invention comprising a system for protecting/controlling access a memory in a computer having a hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instruction, and a software means for responding to that particular indication in which instruction has been translated to host instruction or to a memory mapped I/O device.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or

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on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-9, 12-13 and 18-20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Moore et al. (USPN: 5,437,017), hereinafter Moore.

As per claims 1-2 and 12-13, Moore teaches the invention as claimed including a method and system for protecting memory from being written in a computer which includes a host processor designed to execute instructions of a host instruction set and software for translating instructions from a target instruction set to instructions of the host instruction set comprising:

hardware means for indicating whether a memory address to be written stores a target instruction which has been translated to at least one host instructions is taught as a translation lookaside buffer included in each processor for translating an effective or virtual address to a real address within system memory (e.g. see figure 1; column 4, lines 19 et seq.);

software means responding to an indication ... once the memory address has been written is taught as the processing of a translation lookaside buffer invalidate (TLBI) instruction throughout the multiprocessor data processing system (e.g. see figure 5, column 8, lines 32 et seq.);

As per claim 3, software means for invalidating host instruction translated from target instructions stored at the memory address is clearly taught by Moore as executing the TLBI

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instruction by all processors within the system to maintain coherency (e.g. see abstract, column 3, lines 12 et seq.);

As per claim 5, software means for protecting against writing the memory address removes translations associated with the memory address is taught as means for purging all instructions within the plurality of processors for achieving coherency (e.g. see claims 12 and 13);

As per claim 6, see argument with respect to claim 1, also Moore clearly teaches the hardware means comprise a translation lookaside buffer, and a storage position in each storage location of the translation lookaside buffer (e.g. see figure 1; column 2, lines 7 et seq. and column 6, lines 21 et seq.);

As per claim 7, Moore teaches a computer system comprising: a host processor (e.g. see figure 1); software for translating instructions ... (e.g. see abstract, figure 5); memory for storing target instruction (e.g. see figures 1 or 2); translation lookaside buffer (e.g. see figure 1); hardware means for generating and exception to a write access ... to a host instruction is taught as means for suspending execution of instructions within each of said plurality of processors until coherency is achieved (e.g. see claim 12);

As per claim 8, Moore clearly teaches the hardware means comprise a translation lookaside buffer, and a storage position in each storage location of the translation lookaside buffer

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(e.g. see figure 1; column 2, lines 7 et seq. and column 6, lines 21 et seq.);

As per claim 9, software means responding to an exception to a write ... will not be utilized before being updated is taught as the processing of a translation lookaside buffer invalidate (TLBI) instruction throughout the multiprocessor data processing system (e.g. see figure 5, column 8, lines 32 et seq.);

As per claims 18-20, they encompass the same scope of invention as to that of claims 1-3, it should be noted that the memory controller being claimed in claim 18 in which it comprises a translation lookaside buffer... etc, is equivalent to the memory management unit (MMU) having a TLB (e.g. see figure 3), and other equivalent elements as detailed in claims 1-3. The claims therefore are rejected for the same reason as set forth above. It should be noted that the concept of target instruction being translated into host instruction wherein code intended for a first target processor is translated into code for running on different host processor which is clearly taught by Moore starting on column 4, lines 19 et seq.; for example, Moore does disclose that if the conditional branch is predicted as "taken" then the target instruction is utilized, otherwise it is purged, and the sequential instruction is retrieved.

Conclusion

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7. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

After-final (703) 746-7238

Official (703) 746-7239

Non-Official/Draft (703) 746-7240

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is 703-305-3842.

The examiner can normally be reached on Monday-Thursday from 6:30 AM to 4:00 PM. The examiner can also be reached on alternate Fridays or e-mailed at *tuan.thai@uspto.gov*;

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Matthew M. Kim can be reached on (703) 305-3821.

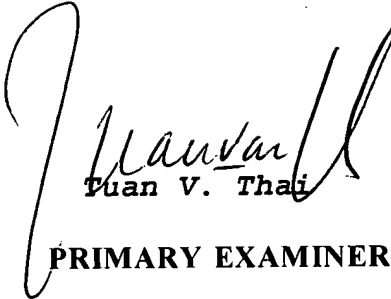
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

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TVT/January 11, 2002


Tuan V. Thai
PRIMARY EXAMINER
Group 2100